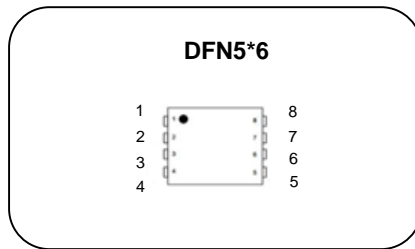


N-channel Enhanced mode DFN5*6 MOSFET

Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 5.9m Ω)@ $V_{GS}=4.5V$
(Typ 4.0m Ω)@ $V_{GS}=10V$
- Low Gate Charge (Typ 38.5nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: Synchronous Rectification, Li Battery Protect Board, Motor Drives



4. Gate 5,6,7,8.Drain 1,2,3.Source

| | |
|--------------|---|
| BV_{DSS} | : 30V |
| I_D | : 70A |
| $R_{DS(ON)}$ | : 5.9m Ω @ $V_{GS}=4.5V$ 4.0m Ω @ $V_{GS}=10V$ |

General Description

This power MOSFET is produced with advanced technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.



Order Codes

| Item | Sales Type | Marking | Package | Packaging |
|------|----------------|------------|---------|-----------|
| 1 | SW HA 041R03VT | SW041R03VT | DFN5*6 | REEL |

Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|-------------|------------|
| V_{DSS} | Drain to source voltage | 30 | V |
| I_D | Continuous drain current (@ $T_C=25^\circ C$) | 70* | A |
| | Continuous drain current (@ $T_C=100^\circ C$) | 46* | A |
| I_{DM} | Drain current pulsed (note 1) | 280 | A |
| I_{DSM} | Continuous drain current (@ $T_a=25^\circ C$) | 22 | A |
| | Continuous drain current (@ $T_a=70^\circ C$) | 18 | A |
| V_{GS} | Gate to source voltage | ± 20 | V |
| E_{AS} | Single pulsed avalanche energy (note 2) | 81 | mJ |
| E_{AR} | Repetitive avalanche energy (note 1) | 8 | mJ |
| dv/dt | Peak diode recovery dv/dt (note 3) | 5 | V/ns |
| P_D | Total power dissipation (@ $T_C=25^\circ C$) | 36 | W |
| | Total power dissipation (@ $T_a=25^\circ C$) | 3.4 | W |
| T_{STG}, T_J | Operating junction temperature & storage temperature | -55 ~ + 150 | $^\circ C$ |

*. Drain current is limited by junction temperature.

Thermal characteristics

| Symbol | Parameter | Value | Unit |
|------------|---|-------|--------------|
| R_{thjc} | Thermal resistance, Junction to case | 3.5 | $^\circ C/W$ |
| R_{thja} | Thermal resistance, Junction to ambient | 36.5 | $^\circ C/W$ |

Note: R_{thja} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{thjc} is guaranteed by design while R_{thca} is determined by the user's board design.



DFN5*6 R_{thja} : 36.5 $^\circ C/W$ on a 1 in² pad of 2oz copper.

Electrical characteristic ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|---|---|----------------------------|------|------|---------------------|
| Off characteristics | | | | | | |
| BV_{DSS} | Drain to source breakdown voltage | $V_{GS}=0V, I_D=250\mu A$ | 30 | | | V |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown voltage temperature coefficient | $I_D=250\mu A$, referenced to 25°C | | 0.02 | | V/ $^\circ\text{C}$ |
| I_{DSS} | Drain to source leakage current | $V_{DS}=30V, V_{GS}=0V$ | | | 1 | μA |
| | | $V_{DS}=24V, T_J=125^\circ\text{C}$ | | | 50 | μA |
| I_{GSS} | Gate to source leakage current, forward | $V_{GS}=20V, V_{DS}=0V$ | | | 100 | nA |
| | Gate to source leakage current, reverse | $V_{GS}=-20V, V_{DS}=0V$ | | | -100 | nA |
| On characteristics | | | | | | |
| $V_{GS(TH)}$ | Gate threshold voltage | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1.0 | | 2.5 | V |
| $R_{DS(ON)}$ | Drain to source on state resistance | $V_{GS}=4.5V, I_D=20A, T_J=25^\circ\text{C}$ | | 5.9 | 7.5 | m Ω |
| | | $V_{GS}=10V, I_D=30A, T_J=25^\circ\text{C}$ | | 4.0 | 5.2 | m Ω |
| | | $V_{GS}=10V, I_D=30A, T_J=125^\circ\text{C}$ | | 6.1 | | m Ω |
| G_{fs} | Forward transconductance | $V_{DS}=5V, I_D=20A$ | | 39.5 | | S |
| Dynamic characteristics | | | | | | |
| C_{iss} | Input capacitance | $V_{GS}=0V, V_{DS}=15V, f=1\text{MHz}$ | | 1962 | | pF |
| C_{oss} | Output capacitance | | | 227 | | |
| C_{rss} | Reverse transfer capacitance | | | 208 | | |
| $t_{d(on)}$ | Turn on delay time | $V_{DS}=15V, I_D=30A, R_G=4.7\Omega, V_{GS}=10V$ (note 4,5) | | 6 | | ns |
| t_r | Rising time | | | 28 | | |
| $t_{d(off)}$ | Turn off delay time | | | 39 | | |
| t_f | Fall time | | | 19 | | |
| Q_g | Total gate charge | $V_{DS}=24V, V_{GS}=10V, I_D=30A, I_G=3\text{mA}$ (note 4,5) | | 38.5 | | nC |
| Q_{gs} | Gate-source charge | | | 5.6 | | |
| Q_{gd} | Gate-drain charge | | | 10 | | |
| R_g | Gate resistance | | $V_{DS}=0V, F=1\text{MHz}$ | | 3.7 | |

Source to drain diode ratings characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------|-----------------------------|---|------|------|------|------|
| I_S | Continuous source current | Integral reverse p-n Junction diode in the MOSFET | | | 70 | A |
| I_{SM} | Pulsed source current | | | | 280 | A |
| V_{SD} | Diode forward voltage drop. | $I_S=45A, V_{GS}=0V$ | | | 1.4 | V |
| t_{rr} | Reverse recovery time | $I_S=15A, V_{GS}=0V, di_f/dt=100A/\mu s$ | | 9.9 | | ns |
| Q_{rr} | Reverse recovery charge | | | | 1.3 | nC |

※. Notes

1. Repeattive rating : pulse width limited by junction temperature.
2. $L=0.5\text{mH}, I_{AS}=18A, V_{DD}=25V, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. $I_{SD} \leq 15A, di/dt = 100A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

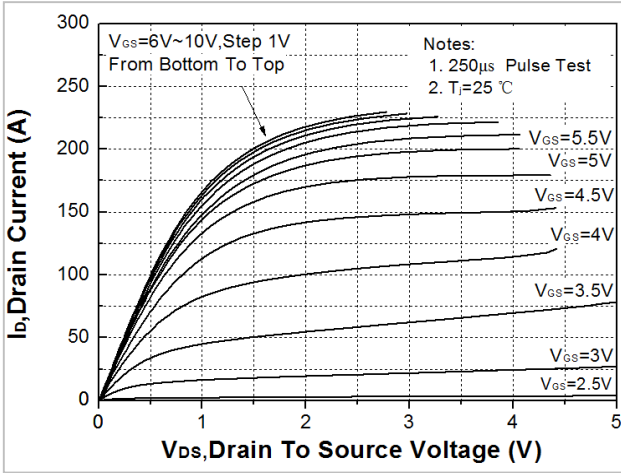


Fig. 2. Transfer Characteristics

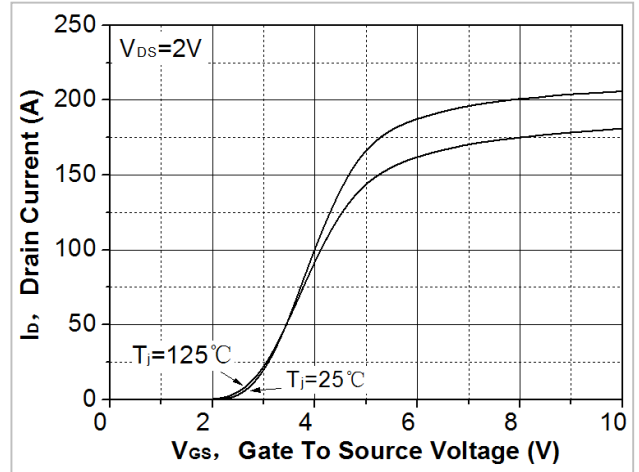


Fig. 3. On-resistance variation vs. drain current and gate voltage

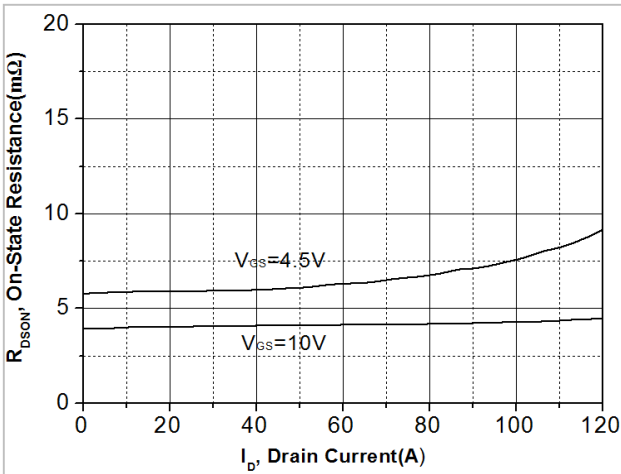


Fig. 4. On-state current vs. diode forward voltage

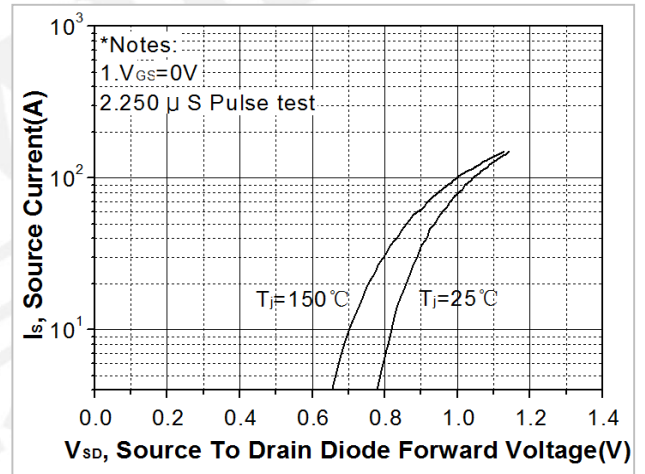


Fig 5. Breakdown voltage variation vs. junction temperature

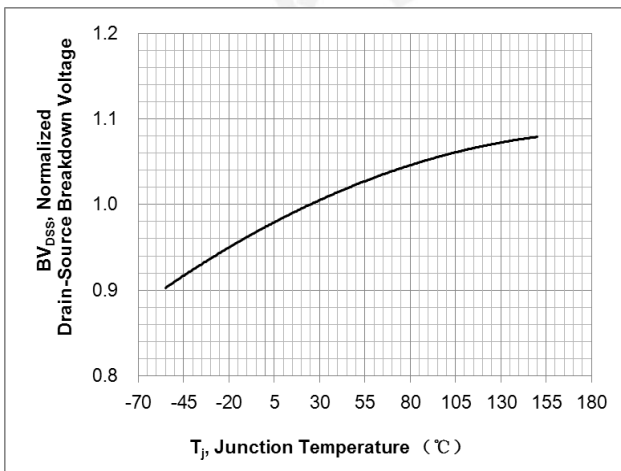


Fig. 6. On-resistance variation vs. junction temperature

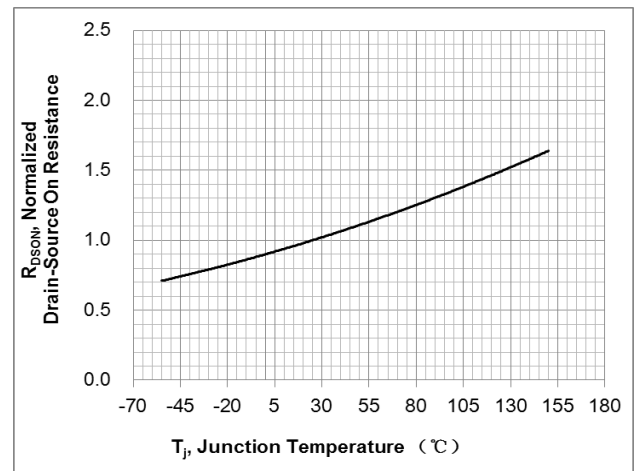


Fig. 7. Gate charge characteristics

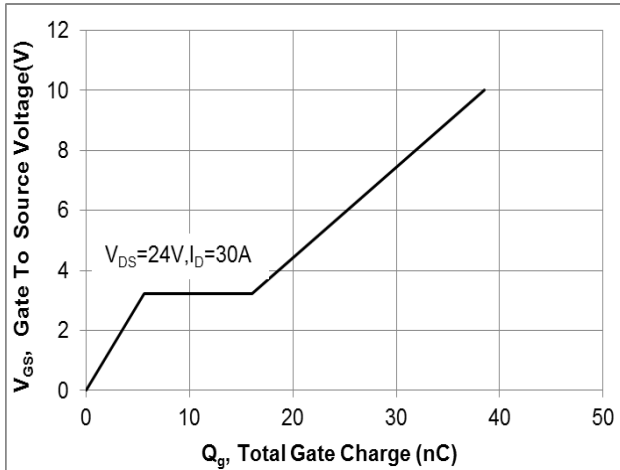


Fig. 8. Capacitance Characteristics

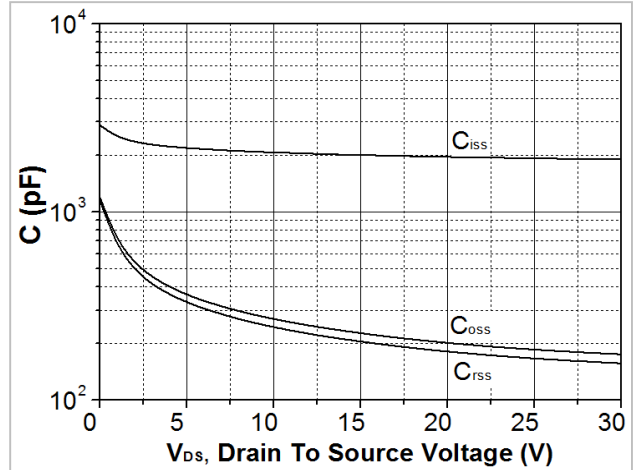


Fig. 9. Maximum safe operating area

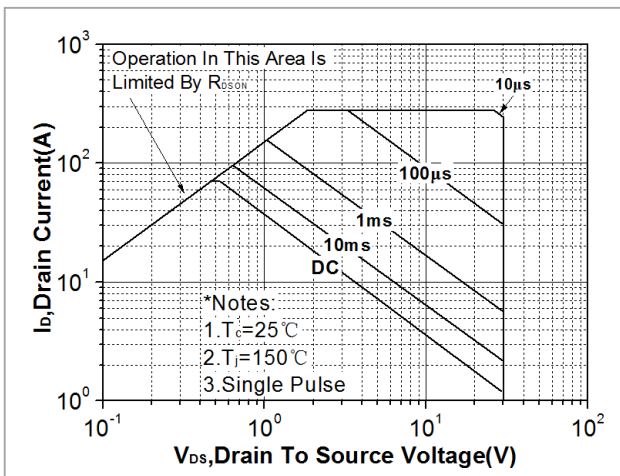


Fig. 10. Maximum drain current vs. case temperature

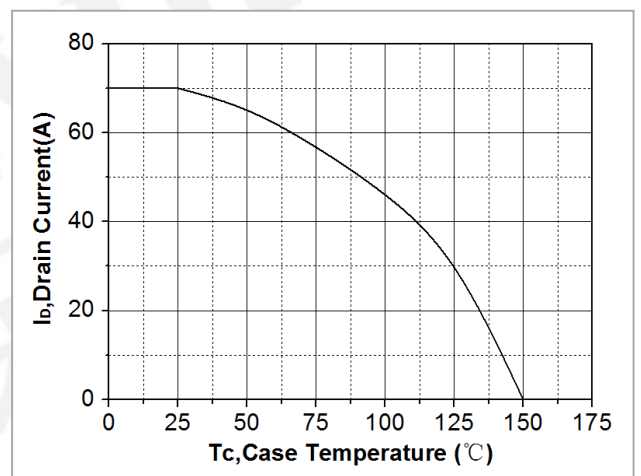


Fig. 11. Transient thermal response curve

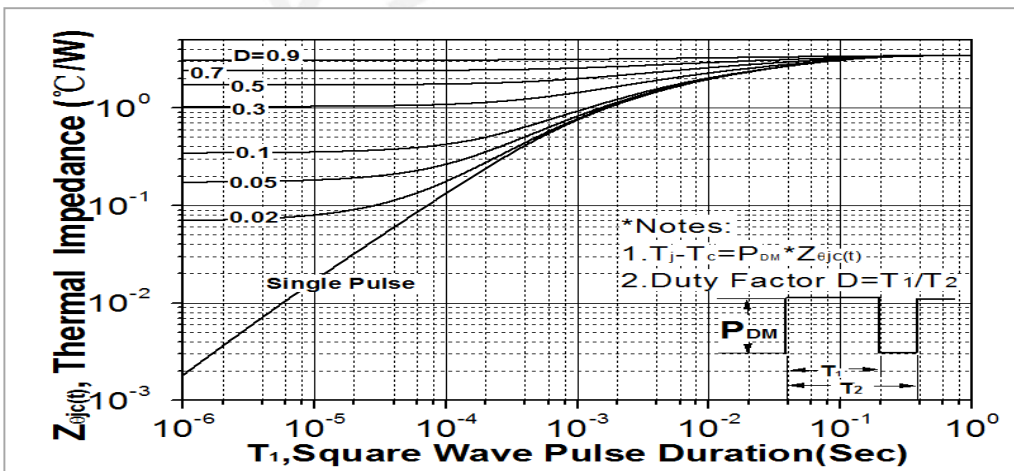


Fig. 12. Gate charge test circuit & waveform

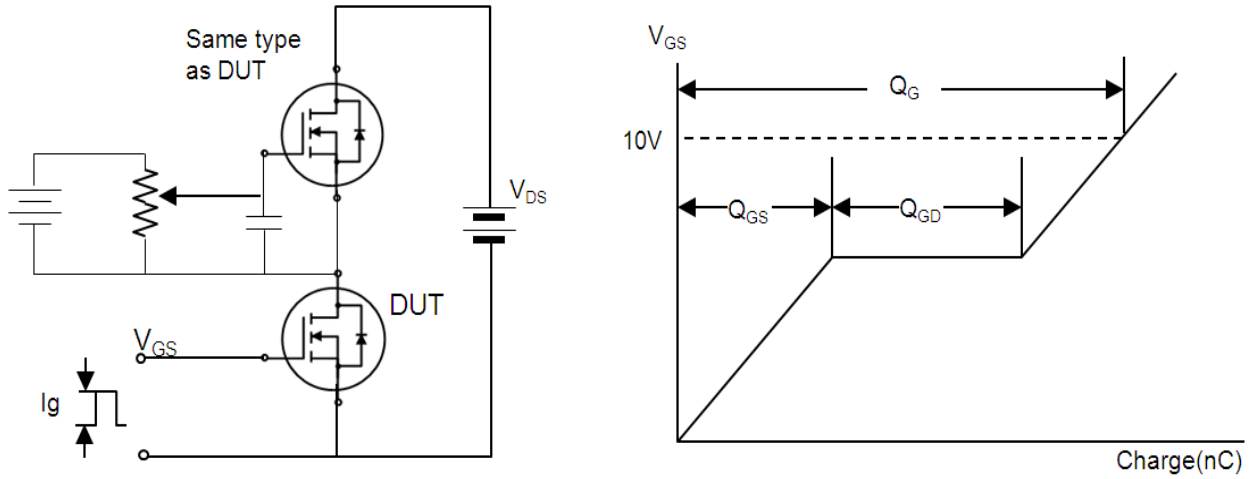


Fig. 13. Switching time test circuit & waveform

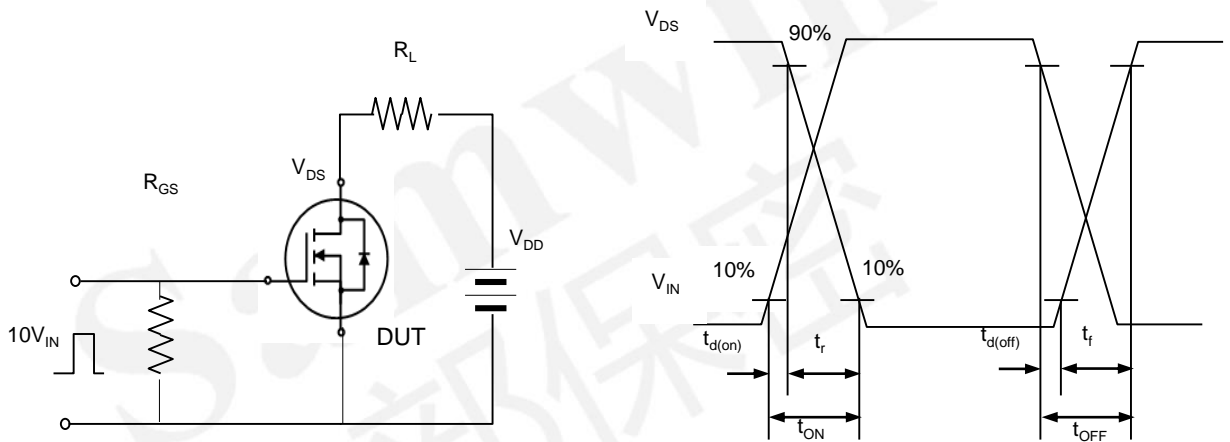


Fig. 14. Unclamped Inductive switching test circuit & waveform

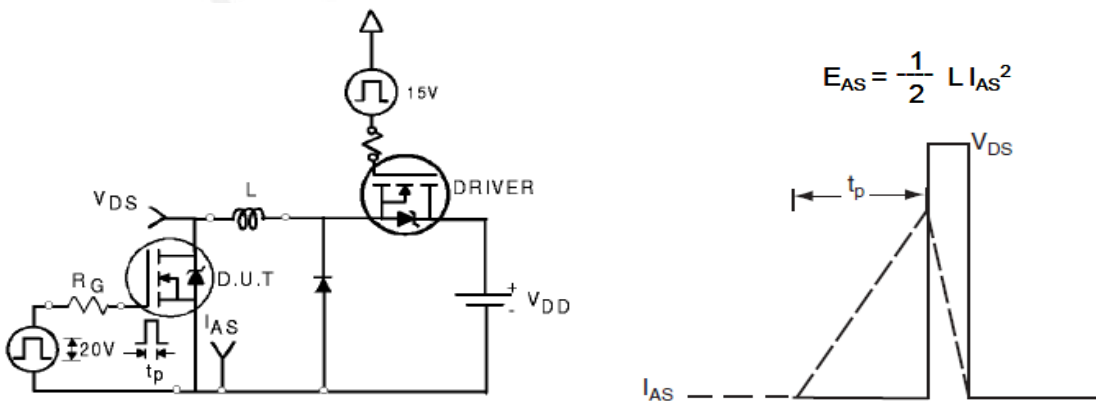
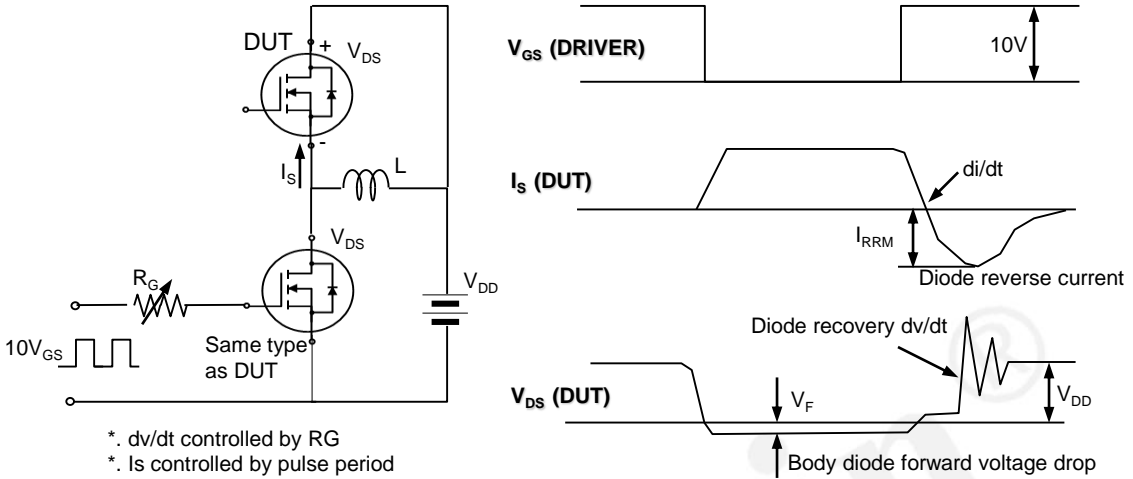


Fig. 15. Peak diode recovery dv/dt test circuit & waveform



DISCLAIMER

* All the data & curve in this document was tested in SEMIPOWER TESTING & APPLICATION CENTER.

* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.

* Qualification standards can also be found on the Web site (<http://www.semipower.com.cn>) 

* Suggestions for improvement are appreciated, Please send your suggestions to samwin@samwinsemi.com